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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/578,314	05/04/2006	Tetsuya Tanaka	P29850	5584

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EXAMINER	
CHERY, MARDOCHEE	

ART UNIT	PAPER NUMBER
2188	

NOTIFICATION DATE	DELIVERY MODE
01/14/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/578,314	TANAKA, TETSUYA	
	Examiner	Art Unit	
	Mardochee Chery	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 May 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/13/06, 8/4/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Oath/Declaration

2. The Oath/Declaration submitted on May 4, 2006 has been reviewed and considered by Examiner.

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on 8/4/06 and 9/13/06 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamazaki (2003/0236947).

As per claim 1, Yamazaki discloses an N-way set-associative cache memory [Fig. 3, *Way 0, Way 1...Way n*] comprising: a control register operable to indicate one or more ways among N ways [Fig. 3, *control register 215*]; a control unit operable to activate the way indicated by said control register [Fig. 3, *Register 215, decoder 216*]; and an updating unit operable to update contents of said control register [Fig. 3, *address register 201, set address 203;* Fig. 4, *updating circuit 301*].

As per claim 2, Yamazaki discloses said control unit is operable to restrict at least replacement, for a way other than the active way indicated by said control register [Fig. 3, replacement control circuit 218; Fig. 4, *replacement object selection circuit 303, replacement way signal, active signal*; pars. 0045-0049].

As per claim 3, Yamazaki discloses a tag holding unit, provided for each of the ways, operable to hold, as a tag, a cache data address [Fig. 3, *cache tag register 205*]; and N-comparison units operable to judge whether a hit or a mishit has occurred [Fig. 3, *comparison circuit 208, Reg 211, hit signal, mishit signal*], by comparing a tag address and N-tags outputted by said tag holding unit [Fig. 3, par. 0031], the tag address being an upper portion of a memory access address outputted from a processor [Fig. 5, par. 0034], wherein said control unit is operable to disable a comparison unit corresponding to a way other than the active way indicated by said control register [Fig. 5, pars. 0036, 0038, 0042].

As per claim 4, Yamazaki discloses said control unit is operable to disable tag outputting to a comparison unit, for a cache address holding unit corresponding to the way other than the active way indicated by said control register [pars. 0013, 0014, 0031, 0048].

As per claim 5, Yamazaki discloses, when a memory access address is outputted from the processor [Fig. 2, *processors 111-122, controllers 113, 123*], said control unit is operable to: control said comparison units to perform, for a maximum of two times, tag comparison for the memory access address [pars. 0031, 0034, 0035]; disable, in a first tag comparison, a comparison unit corresponding to the way other than the active way indicated by said control register [Fig. 5, pars. 0036, 0038, 0042]; and cause said comparison units to perform a second comparison, without disabling the

comparison unit corresponding to the way other than the active way, in the case where it is judged that a mishit has occurred in the first tag comparison [Fig. 5, pars. 0036, 0038, 0042].

As per claim 6, Yamazaki discloses said control unit is operable to disable, in the second tag comparison, the comparison unit corresponding to the way other than the active way [pars. 0013, 0014, 0031, 0048].

As per claim 7, Yamazaki discloses said control unit is operable to prohibit status updating for the way other than the active way indicated by said control register [par. 0012].

As per claim 8, Yamazaki discloses said control unit is operable to prohibit updating of information indicating an access order of the way other than the active way indicated by said control register [par. 0012].

As per claim 9, Yamazaki discloses a reset unit operable to reset the information indicating an access order for the ways, when the contents of said control register are updated by said updating unit [Figs. 4-5, set address 0-255, active signal 401].

As per claim 10, Yamazaki discloses the information indicating the access order is 1-bit data for each cache entry [par. 0045], said cache memory further comprises a

register operable to hold data indicating a round position for selecting, in a round robin, one way from a plurality of replaceable ways, and said reset unit is operable to reset said register when the contents of said control register are updated by said updating unit [pars. 0045, 0046].

As per claim 11, Yamazaki discloses said updating unit includes: a holding unit operable to hold way data for respective tasks, which specifies a way to be activated; and a rewriting unit operable to rewrite said control register so as to hold way data corresponding to a task being executed [pars. 0045, 0046; claim text 4].

As per claim 12, Yamazaki discloses said holding unit is operable to hold the way data as part of context data for the respective tasks which is stored in a memory [Fig. 3, *registers 205, 212, 206, 213*], and during task switching, said rewriting unit is operable to save, in the memory, way data of a current task, inside said register, and to restore, from the memory to said control register, way data of a next task [Fig. 3, *registers 206, 213*].

As per claim 13, Yamazaki discloses said holding unit is operable to hold the way data for the respective tasks [Fig. 3, *registers 205, 212, 206, 213*], and said rewriting unit includes: an address storage unit operable to store an address range of the respective tasks, stored in the memory [Fig. 3, address register 201]; an identification unit operable to identify the task being executed, based on the address range stored in the address

storage unit and an instruction fetch address outputted from a processor [Fig. 3, *comparison circuit 208, Reg 211, hit signal, mishit signal*]; and a selection unit operable to select, from said holding unit, way data corresponding to the identified task being executed [Fig. 3, *Selection unit 217*].

As per claim 14, Yamazaki discloses said holding unit is operable to hold the way data for the respective tasks [Fig. 3, *registers 205, 212, 206, 213*], said rewriting unit includes: a selection unit operable to select way data from said holding, according to a task number outputted from a processor unit, the way data corresponding to a task being executed [Fig. 3, *selection unit 217, replacement control circuit 218*]; and a writing unit operable to write the selected way data into said control register [Fig. 3, *replacement control circuit 218*].

As per claim 15, Yamazaki discloses way data held in said holding unit is assigned to a task, by an operating system [page 4, text claim 2].

As per claim 16, Yamazaki discloses a unit of replacement for respective ways can be switched between a line size of a cache entry and a size which is one over two to the nth power of the line size, said control register is further operable to indicate a replacement size for respective tasks, and said control unit is operable to perform replacement control with the replacement size indicated by said control unit [par. 0027].

As per claim 17, Yamazaki discloses said control unit is operable to restrict at least replacement for a way other than the active way indicated by said control register, and to perform replacement on the active way indicated by said register, with the size indicated by said control register [par. 0012].

As per claim 18, Yamazaki discloses said updating unit includes: a holding unit operable to hold way data for respective tasks, specifying a way to be activated, and the replacement size for the respective tasks [Fig. 3, *comparison circuit 208, Reg 211, hit signal, mishit signal*]; pars. 0045, 0046; and a rewriting unit operable to rewrite said control register so as to hold way data and a replacement size corresponding to a task being executed [Fig. 3, *replacement control circuit 218*].

As per claim 19, Yamazaki discloses a storage unit operable to store, for each cache entry, 1-bit access information indicating whether or not the cache entry has been accessed, the cache entry holding data which is a unit of caching [para. 0045, 0046]; and a selection unit operable to select a cache entry to be replaced from among cache entries corresponding to access information indicating that a cache entry has not been accessed [Fig. 3, *selection unit 217, replacement control circuit 218*].

As per claim 20, Yamazaki discloses a register operable to hold data indicating a round position for selecting, in a round robin, one way from a plurality of ways that can be replaced [pars. 0045, 0046]; and a reset unit operable to reset, when the contents of

said control register are updated by said updating unit, information indicating an access order for ways, and the data, in said register, indicating the round position [pars. 0045, 0046].

As per claim 21, Yamazaki discloses a control method for controlling an N-way set-associative cache memory, comprising: a step of setting [Fig. 4, *set address*], to a control register [Fig. 4, *control register 302*], way data indicating one or more ways among N ways [Fig. 4, *way data 0-255*]; and a control step of activating the way indicated by the control register [Fig. 4, *active signal, replacement object selection circuit, replacement way signal*].

As per claim 22, Yamazaki discloses wherein in said controlling, at least replacement is restricted for a way other than the active way indicated by the control register [par. 0012]

As per claim 23, Yamazaki discloses an updating step of reading-out, from a holding unit, way data corresponding to a task being executed, and writing the read-out way data into the control register, the holding unit holding way data for respective tasks, the way data specifying a way to be activated [Fig. 3, pars. 0045, 0046].

Conclusion

6. When responding to the office action, Applicant is advised to clearly point out the patentable novelty that he or she thinks the claims present in view of the state of the art disclosed by references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111(c).

7. When responding to the Office action, Applicant is advised to clearly point out where support, with reference to page, line numbers, and figures, is found for any amendment made to the claims.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mardochee Chery whose telephone number is (571) 272-4246. The examiner can normally be reached on 8:30A-5:00P.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung Sough can be reached on (571) 272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

January 6, 2007

Mardochee Chery
Examiner
AU: 2188

HYUNG S. SOUGH
SUPERVISORY PATENT EXAMINER
01/07/08